

Response under 37 CFR 1.116  
Technology Center - 2815  
42P12399

**Amendments to the Claims**

1. (currently amended) A memory device comprising[[:]]

a power supply in package (PSIP) device comprising

an integrated circuit die including a memory array and having a first surface;

a voltage regulator circuit; and

a passive component of ~~a charge pump~~ the voltage regulator circuit, wherein the passive component is mounted overlying the first surface of the integrated circuit die and electrically coupled to the integrated circuit die, ~~the charge pump~~ voltage regulator circuit to provide a programming voltage potential to the memory array.

2. (Original) The memory device of claim 1, wherein the passive component is mounted to the integrated circuit die with an epoxy material.

3. (Original) The memory device of claim 2, wherein the epoxy material between the passive component and the integrated circuit die is less than about 0.050 millimeters in thickness.

4. (Original) The memory device of claim 1, wherein the passive component is mounted to the integrated circuit die with a conductive material.

Response under 37 CFR 1.116  
Technology Center - 2815  
42P12399

5. (currently amended) The memory device of claim 1, wherein the passive component includes at least one of a capacitor [[or]] and an inductor.

6. (Original) The memory device of claim 1, further comprising:  
a substrate, wherein the integrated circuit die is mounted to the substrate.

7. (Original) The memory device of claim 6, wherein the integrated circuit is mounted to the substrate with a non-conductive material.

8. (Original) The memory device of claim 6, further comprising a first wire bond electrically coupling at least a portion of the integrated circuit to the substrate.

9. (Original) The memory device of claim 8, further comprising a second wire bond electrically coupling at least a portion of the passive component to the substrate.

10. (Original) The memory device of claim 8, further comprising a second wire bond electrically coupling at least a portion of the passive component to the integrated circuit die.

11. (Original) The memory device of claim 1, wherein the integrated circuit die includes a flash memory array.

12. (cancelled)

Response under 37 CFR 1.116  
Technology Center - 2815  
42P12399

13. (currently amended) A method comprising[[:]]  
making a device comprising a power supply in package (PSIP) device by:  
forming a substrate;  
mounting an integrated circuit die on said substrate;  
mounting a passive component of a charge pump voltage regulator circuit,  
the passive component mounted overlying the substrate; and  
electrically coupling the passive component to at least a portion of the  
integrated circuit die.

14. (Original) The method of claim 13, further comprising adhesively attaching  
the passive component to the integrated circuit die.

15. (Original) The method of claim 14, further comprising adhesively attaching  
the passive component to the integrated circuit die with a non-conductive adhesive.

16. (Original) The method of claim 13 including wire bonding the passive  
component to the substrate.

17. (Original) The method of claim 13 including wire bonding the passive  
component to the integrated circuit die.

18-20. (cancelled)

Response under 37 CFR 1.116  
Technology Center - 2815  
42P12399

21. (new). The apparatus of claim 1, wherein the memory device further comprises an encapsulant at least partly encapsulating the integrated circuit die and the passive component.

22. (new) The method of claim 13, further comprising molding the die and the passive component in an encapsulant.